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SUBSTITUTE SPECIFICATION

LEVEL TRANSFORMING CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a level transforming circuit serving as an interface of a digital circuit, wherein the level transforming circuit operates with different electricity source voltages.

2. Description of Related Art

The finer the structure of a MOS transistor becomes, the weaker the strength of a gate oxide film becomes. For example, a MOS transistor produced in a fine process of an extent of $0.35\ \mu\text{m}$ is able to operate at an electricity source voltage of an extent of 3.3V. Further, a MOS transistor produced in a latest fine process of an extent of $0.18\ \mu\text{m}$ is able to operate at an electricity source voltage of an extent of 1.8V. In the conventional art, when it is necessary to make an interface between a circuit of $0.18\ \mu\text{m}$ fine process and a circuit of $0.35\ \mu\text{m}$ fine process, a level transforming circuit in the interface required both MOS transistors of 1.8V and 3.3V.

(First prior art)

Fig. 10 is a circuit diagram showing a structure of a level transforming circuit of a first prior art disclosed in Japanese patent publication No. 4-150411. This level transforming circuit comprises, as shown in Fig. 10, a latch circuit 200, which operates with a high voltage electricity source VDD (3.3V). NMOS 211 and 212 are connected between node N11, N12 of this latch circuit 200 and the ground. A signal IN from a circuit which operates with a low voltage electricity source VCC (1.8) is impressed to the gate of NMOS 211. On the other hand, an inverse signal of the